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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SE00/00850	May 3, 2000	May 4, 1999

TITLE OF INVENTION
SWITCH APPARATUS

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated/ Elected Office (DO/EO/US) the following items under 35 U.S.C. 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the international Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureaus.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 37(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (not executed).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☐ Other items or information:

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INTERNATIONAL APPLICATION NO. PCT/SE00/00850	INTERNATIONAL FILING DATE May 3, 2000	JC13 Rec'd PCT/PTO 22 OCT 2001

17. ☒ The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS				
(1)FOR	(2)NUMBER FILED	(3)NUMBER EXTRA	(4)RATE	(5)CALCULATIONS
TOTAL CLAIMS	10 -20	0	X $18.00	$ 0.00
INDEPENDENT CLAIMS	2 -3	0	X $84.00	0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$ 280.00

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)): **CHECK ONE BOX ONLY** ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00	
☐ No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $740.00	
☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00	$ 1,040.00
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4) $100.00	
☐ Filing with EPO or JPO search report $890.00	
Surcharge of $130.00 for furnishing the National fee or oath or declaration later than 20 30 mos. from the earliest claimed priority date (37 CFR 1.492(e)).	
1 TOTAL OF ABOVE CALCULATIONS	= 1,320.00
Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (Note 37 CFR 1.9, 1.27, 1.28).	- $ 660.00
SUBTOTAL	= 660.00
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0 TOTAL FEES ENCLOSED	$ 660.00

a. ☐ A check in the amount of $___ to cover the above fees is enclosed.

b. ☒ Please charge Deposit Account No. 16-1150 in the amount of $ 660 to cover the above fees. A copy of this sheet is enclosed.

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18. ☐ Other instructions

n/a

19. ☒ All correspondence for this application should be mailed to

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NEW YORK, N.Y. 10036-2711

20. ☒ All telephone inquiries should be made to (212) 790-9090

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SWITCH APPARATUS

Technical Field and Background of the Invention

The present invention refers the field of data and telecommunications, and more specifically to an apparatus in which a number of switch elements are combined into forming a larger scale switch.

When designing and operating communication networks and components, there are many situations in which scalability when it comes to switching capacity and flexibility is of great advantage. The option of handling smaller switch elements that, if necessary or desired, may be combined into forming larger switches with greater capacity allows greater design freedom and simplifies product logistics.

When for example using a 4×4 (4 input ports and 4 output ports) switch element as building block, an 8×8, as wll as a 16×16 or 32×32 switch can be built based thereupon. Thus, instead of designing, producing, and logistically handling and supporting four different swtch architectures, only one scaleable architecture would require such attention.

Similarly, scalability when operating products in larger networks has the advantage of lowering operating cost and simplifying design and operation as one product can be configured for use in many different situations having different switching requirements.

A disadvantage with prior art schemes for combining switch elements into forming lager scale switches is that they a) often require complex interconnecting and configuration schemes, b) require internal modification of the individual switch elements, or c) do not combine the individual switch element into a switch that offers non-blocking operation.

Summary of the Invention

An object of the invention is to provide a switch architecture in which a number of switch elements are combined into forming a larger scale switch and in which interconnections and configurations of the switch elements are simple, requires little or no internal configuration of the individual switch elements, and results in a switch that offers non-blocking operation.

This and other object are achieved by the invention as defined in the accompanying claims.

The invention is based upon the use of a switch element in which the relationship between an output port and each one of one or more input ports thereof is such that time-switching is performed, according to switch instructions provided by a control unit, with respect to one or more slots that are received at the respective input port and that are to be switched to the output port, and in which the relationship between said output port and an additional input port is such that no time-switching is performed with respect to slots that are received at said additional input port and that are switched to said output port.

Furthermore, the invention defines ways in which switch elements of this kind are to be interconnected to form larger scale switches, using said additional port as means for interconnecting the switch elements. Typically, said additional port is used to receive an input from another switch element, said input already having been at least time-switched by said another switch element.

According to a preferred embodiment, each switch element comprises, for each one of said one or more in put ports, a second additional output port, referred to as repeat port, wherein data received at the respective one of said one or more input ports is transmitted from the respective repeat port as received at the respective input port, thereby making it possible to provide an

input signal to several switch elements by connecting them in series using said repeat port.

According to another preferred embodiment, the switch elements of the invention are arranged to receive and transmit data in essentially equally sized, e.g. 125 µs, frames, said frame typically being divided into fixed size, e.g. 64-bit, time slots. Furthermore, the data transfer within and between the switch elements that form a larger scale switch according to the invention is also preferably performed in the context of frames of data. For example, the invention will be applicable for building switches in so-called DTM (Dynamic synchronous Transfer Mode) networks. For further information on such a network, reference is made to "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994.

To further exemplify and describe a preferred way in which time and, optionally, space switching is performed in said switch element with respect to said one or more input ports, reference is made to the not yet published Swedish Patent Application 9704067-9.

The above mentioned features, embodiments and aspects of the invention will now be further exemplified with reference to the accompanying drawing.

Brief Description of the Drawings

Exemplifying embodiment of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows an embodiment of a switch element of the kind used to build larger scale switches according to the invention;

Fig. 2 schematically shows an example on the design of the time-switching circuit illustrated in Fig. 1;

Fig. 3 schematically shows an embodiment of a switch that is built up by interconnected switch elements of the kind shown in Fig. 1;

Fig. 4 schematically shows the switch of Fig. 3 according to a modified embodiment;

Fig. 5 schematically shows another embodiment of a switch element of the kind used to build larger scale switches according to the invention;

Fig. 6 schematically shows an embodiment of a switch that is built up by interconnected switch elements of the kind shown in Fig. 5;

Figs. 7A and 7B schematically shows sixteen 4x4 switch elements that are combined into forming a 16x16 switch.

Detailed Description of Preferred Embodiment

An exemplifying embodiment of a switch element of the kind used to build larger scale switches according to the invention will now be describe with reference to Fig. 1. In Fig. 1, the switch element 100 comprises a first input port 110, a second input port 120, a time-switching circuit 130, a selecting multiplexor 140, and an output port 150.

In operation, the first input port 110 will typically be connected to receive data in essentially fixed sized frames that are divided into fixed sized slots. For exemplifying purposes, it will throughout the drawings be assumed that the frame length is 125 μs and that each slot comprises 64 bits of data. The frames received via the input port 110 are forwarded to the time-switching circuit 130. The time-switching circuit 130 is arranged to provide for time-switching of the slots of each received frame, in accordance with time-switching instructions provided by a switching control unit (not shown), to provide an output frame of slots to the selecting multiplexor 140. An example on the design of the time-switching

circuit will be described more in detail below with reference to Fig. 2.

In parallel, the second input port 120 will optionally be connected to receive data in similar, essentially fixed sized frames. However, the frames of data that are received via the second input port 120 are forwarded directly to the selecting multiplexor 140, i.e. with the time sequential order of the slots of each frame maintained.

Consequently, if both input ports of the switch element 100 are connected to receive frames of data, the selecting multiplexor will simultaneously be provided with a) frames from the time-switching circuit 130, the slots of the frames having been time-switched as compared to their locations in the frames when received at the input port 110, and b) frames from the second input port, the time slots thereof not having been time-switched.

The selecting multiplexor 140 is arranged to output frames that are to be transmitted from the output port 150 of the switch element 100 by selectively, in accordance with switching instructions provided by the above-mentioned switching control unit, combining slots of frames received from the time-switching circuit 130 with slots of frames received directly from the second input port 120. In the exemplifying embodiment illustrated in Fig. 1, the selecting multiplexor 140 is arranged to select, for each slot forwarded to the output port 150, either a slot received from the time-switching circuit 130 or a slot received from the second input port 120. More specifically, as the n:th time slot of a frame that is currently forwarded to the output port 150, the selecting multiplexor 140 will select either the n:th slot of the frame that is currently received from the time-switching circuit 130 or the n:th slot of the frame that is currently received from the second input port 120. To be noted, if the second input port 120 is not connected to receive any input signal, the selecting

multiplexor will be instructed to simply forward the entire frames of slots as received from the time-switching circuit 130.

As will be illustrated more in detail below, when combining the switch element 100 with additional similar switch elements to build a larger scale switch, the first input port 110 will typically be connected to receive an input signal of the larger scale switch and the second input port 120 will be either not connected to receive any signal at all or connected to an output port of another switch element forming the larger scale switch. Consequently, an input port having a non time-switching function and being used to provide for connection to output ports of other switch elements of a larger scale switch, like the input port 120, will sometimes be referred to below as a cascade input port.

An example on the design of the time-switching circuit 130 shown in Fig. 1 will now be described with reference to Fig. 2.

In Fig. 2, the time-switching circuit 130 is arranged to perform time-switching with respect to slots of frames received as input 209 (from port 110 in Fig. 1) to provide output frames as output 231 (to port 150 in Fig. 1). The input frames 209 are provided to a demultiplexor 210. At the same time, a frame synchronization signal 208, which defines the start of each frame received as input 209, synchronizes the operation of an input slot counter 240 and a write buffer selecting unit 250. The write buffer selecting unit 250 is arranged to control the demultiplexor 210, at the rate of the frame synchronization signal, to have it forward each frame of the input 209 sequentially to one of three frame buffers 220a, 220b, and 220c of a frame memory 220 in a modulo-3 fashion. At the same time, the input slot counter 240 controls which entry of the buffer that each specific slot of the frame is written into. The input slot counter 240 is reset on each reception of the frame synchroniza-

tion signal 208 and counts, at the rate of a slot frequency, from a first entry to a last entry of the buffer in sequential order, the slots of each frame thereby being written into the frame buffer to be located therein with maintained sequential slot order.

On the output side, an output frame synchronization signal 232 is used to synchronize operation of an output slot counter 260 and a read buffer selecting unit 270. The output slot counter 260 is reset on each reception of the output frame synchronization signal 232 and counts, at the rate of a slot frequency, to address a first entry to a last entry of a slot mapping table 280 (which may be said to in part form the above-mentioned switching control unit) in sequential order, thus stepping through the slot mapping table once for each output frame. For each specific output slot, the output slot counter 260 will point at a respective entry of the slot mapping table 280. The slot mapping table 280 in turn provides, at each entry, a respective address to the frame memory 220, designating from which entry thereof that slot data is to be retrieved. The entries of the slot mapping table 280 thus define the desired time-switching of the input frame. At the same time, the read buffer selecting unit 270 controls, via the multiplexor 230, from which one of the three frame buffers 220a, 220b, and 220c that slot data is currently to be forwarded, stepping through the three buffers in a modulo-3 fashion at the rate of the output frame synchronization signal 232. As is understood, the function of the write and read buffer selection units 250 and 270 is to make sure that a stored frame is not overwritten until it has been properly read.

An exemplifying embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 1 will now be described with reference to Fig. 3. In Fig. 3, the switch 300 is arranged to perform time and space switching from a first 310 and a second 320 input signal to a first 330 and a

second 340 output signal, all being assumed to be formed by fixed size frames that are divided into fixed size slots. For that purpose, the switch comprises four switch elements 100a-100d of the kind described above with reference to Fig. 1.

As is illustrated, the first input port 110a of the first switch element 100a and the first input port 110b of the second switch element 100b are connected to receive the first input signal 310. Similarly, the first input port 110c of the third switch element 100c and the first input port 110d of the fourth switch element 100d are connected to receive the second input signal 320.

To cascade the switch elements, the output port 150a of the first switch element 100a is connected to the second input port 120c of the third switch element 100c, and the output port 150b of the second switch element 100b is connected to the second input port 120d of the fourth switch element 100d. To be noted, as the first 100a and second 100b switch elements do not have and cascaded inputs, the second input ports 120a, 120b thereof are not connected to receive any input signals.

The first and second output signals 330 and 340 are thereby provided as the output from the output port 150c of the third switch element 100c and the output port 150d of the fourth switch element 100d.

In the switch 300 of Fig. 3, the time-switching circuit 130a of the first switch element 100a will be configured to perform all time-switching necessary with respect to slots of the first input signal 310 that are to be transmitted in frames of the first output signal 330. Similarly, the time-switching circuit 130b of the second switch element 100b will be configured to perform all time-switching necessary with respect to slots of the first input signal 310 that are to be transmitted in frames of the second output signal 340. The so time-switched frames of the first input signal 310 are then forwarded to the selecting multiplexors 140c and 140d of

the third and fourth switch element 100c and 100d, respectively using the cascade input ports 120c and 120d.

In addition, the time-switching circuit 130c of the third switch element 100c will be configured to perform all time-switching necessary with respect to slots of the second input signal 320 that are to be transmitted in frames of the first output signal 330, and the time-switching circuit 130d of the fourth switch element 100d will be configured to perform all time-switching necessary with respect to slots of the second input signal 320 that are to be transmitted in frames of the second output signal 340. The so time-switched frames of the second input signal 320 are thus also forwarded to the selecting multiplexors 140c and 140d of the third and fourth switch element 100c and 100d, respectively.

The selecting multiplexor 140c will then form the first output signal 330 by selecting slots from the first input signal 310 as received via the time-switching circuit 130a and the second input signal 320 as received via the time-switching circuit 130c. Similarly, the selecting multiplexor 140d will form the second output signal 340 by selecting slots from the first input signal 310 as received via the time-switching circuit 130b and the second input signal 320 as received via the time-switching circuit 130d.

An alternative embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 1 is shown in Fig. 4. In the switch 400 of Fig. 4, each switch element 100a-100d is provided with a respective so-called repeat port 125a-125d. The repeat port of a switch element has the function of simply forwarding any data that is received via the first input port of the respective element. Then, instead of connecting an input signal (such as the input signal 310 in Fig. 3) directly to first input ports of two different switch element (such as 100a and 100b in Fig. 3), the input signal is only connected to the input

port of one of these two elements, the other one of the two elements simply being provided with the input signal by having its first input port connected to the repeat port of the first element.

For example, in Fig 4, the first input port 110b of the second switch element 100b receives the first input signal 310 by being connected to the repeat port 125a of the first switch element 100a, and the first input port 110d of the fourth switch element 100d receives the second input signal 320 by being connected to the repeat port 125c of the third switch element 100c. To be noted, as the input signals 310 and 320 are in this example not to be forwarded to any switch elements in addition to the ones shown in the figure, the repeat ports of the second 100b and fourth 110d switch elements are in this case not connected to forward any signals to other switch elements. With the exemption of this use of the repeat ports, the design and operation of the switch 400 of Fig. 4 is the same as the design and operation of the switch 300 of Fig. 3.

Another exemplifying embodiment of a switch element of the kind used to build larger scale switches according to the invention will now be describe with reference to Fig. 5. In Fig. 5, the switch element 500 comprises a first 510, a second 520, a third 511, and a fourth 521 input port, a first 530 and a second 531 time-and-space-switching circuit, a first 540 and a second 541 selecting multiplexor, and a first 550 and a second 551 output port.

The first switching circuit 530 is arranged to provide for time-and-space-switching of slots of frames received via the first input port, in accordance with time-and-space-switching instructions provided by a switching control unit (not shown), to provide an output frame of slots to the first multiplexor 540, and an output frame of slots to the second multiplexor 541. Similarly, the second switching circuit 531 is arranged

to provide for time-and-space switching of slots of frames received via the third input port 511, in accordance with time-and-space-switching instructions provided by a switching control unit (not shown), to also provide an output frame of slots to the first multiplexor 540, and an output frame of slots to the second multiplexor 541. As understood, the design and operation of each one of the time-and-space-switching circuits 530, 531 may be similar to the circuit described above with reference to Fig. 2. For example, the frame memory illustrated in Fig. 2 could simply be provided with an additional read port, output multiplexor and slot selecting mechanism to provide the desired additional output signal.

In parallel, the second 520 and the fourth 521 input port will optionally be connected to forward frames as received directly to the multiplexor 540 and 541, respectively, i.e. with the time sequential order of the slots of each frame maintained.

Each one of the selecting circuits 540, 541 is then arranged to output frames that are to be transmitted from the respective output port 550, 551 by selectively, in accordance with switching instructions provided by a switching control unit (not shown), combining the slots of frames received a) from the circuit 530, b) from the circuit 531, and c) directly from the respective cascade input port 520, 521. For example, in the exemplifying embodiment illustrated in Fig. 5, the selecting circuit 540 is arranged to forward, as the n:th time slot of a frame that is currently forwarded to the output port 550, either the n:th slot of the frame that is currently received from the circuit 530, the n:th slot of the frame that is currently received from the circuit 531, or the n:th slot of the frame that is currently received directly from the input port 520.

An exemplifying embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 5 will now be

described with reference to Fig. 6. In Fig. 6, the switch 600 is arranged to perform time and space switching from frames of four input signals 610-640 to frames of four output signals 650-680 and comprises said four switch elements 500a-500d of the kind described with reference to Fig. 5.

As shown in Fig. 6, the first input port of the first element 500a and the first input port of the second element 500b are connected to receive the first input signal 610, the third input port of the first element 500a and the third input port of the second element 500b are connected to receive the second input signal 620, the first input port of the third element 500c and the first input port of the fourth element 500d are connected to receive the third input signal 630, and the third input port of the third element 500a and the third input port of the fourth element 500d are connected to receive the fourth input signal 640.

To cascade the elements 500a-500c into forming the larger scale switch 600, the first and second output port of the first element 500a is connected to the second and fourth input port, respectively, of the third element 500c, and the first and second output port of the second element 500b is connected to the second and fourth input port, respectively, of the fourth element 500d.

The first 650, second 660, third 670 and fourth 680 output signal is thereby provided as the output from the first output port of the third element 500c, the second output port of the third element 500c, the first output port of the fourth element 500d, and the second output port of the fourth switch element 500d, respectively.

To exemplify the configuration of the switching and multiplexing circuits of the elements 500a-500c when switching time slot from frames of the four input signals 610-640 to, for example, the first output signal 650, the first time-and-space-switching circuit of the first switch element 500a will be configured to perform all

time-switching necessary, with respect to slots of the first input signal 610 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the first switch element 500a. Similarly, the second time-and-space-switching circuit of the first switch element 500a will be configured to perform all time-switching necessary, with respect to slots of the second input signal 620 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the first switch element 500a. The first multiplexor of the first switch element 500a will in turn be configured perform all space selection necessary, with respect to slots of the first 610 and the second 620 input signal that are to be transmitted in frames of the first output signal 650, when providing its output to the first cascade input of the third switch element 500c.

In the switch element 500c, the first time-and-space-switching circuit thereof will be configured to perform all time-switching necessary, with respect to slots of the third input signal 630 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor. Similarly, the second time-and-space-switching circuit of the third switch element 500c will be configured to perform all time-switching necessary, with respect to slots of the fourth input signal 640 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the third switch element 500c. Finally, the first multiplexor of the third switch element 500a will be configured to perform all space selection necessary among frames received from the first switching circuit (referring to input signal 630), the second switching circuit (referring to input signal 640), and the clustered input port (referring to input signals 610 and 620) to provide the desired output signal 650.

To further illustrate the cascading possibilities provided by the invention, Fig. 7A illustrate a 4x4 switch element, sixteen of which having been combined in Fig. 7B into forming a 16x16 switch.

As is shown in Fig. 6A, the switch element has four signal inputs, four signal outputs, four cascade inputs and four repeat outputs. The design and operation of this switch element could for example be similar to the design and operation of the element 500 described above with reference to Fig. 5 by merely adding thereto two additional input port pairs, two switching circuits, two multiplexors, and two output ports, and by providing each one of the then four switching circuits of the element with the capability of providing frames of time switched slots to all four multiplexors of the element, each multiplexor thus selecting time slots among frames provided by the four switching circuits and a respective one of the cascade input ports.

To be understood, even though the invention primarily addresses so-called symmetric or quadratic switch element configurations, for example as illustrated in Figs 3, 7, and 7B, also asymmetric switch element configurations can be envisaged.

Even though exemplifying embodiment of the invention has been described in detail above, modifications, combinations and alterations thereof may be made, as will be clear to those skilled in the art, within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. An apparatus for time and space switching data from a first and a second input signal to a first and a second output signal, said apparatus comprising at least four switch elements (100; 500), each having a first (110; 510) and a second (120; 520) input port and an output port (150; 550) and comprising:

switching means (130; 530) arranged to provide for time-switching of data received from said first input port to provide an output referring to said output port; and

selecting means (140; 540) for defining a signal to be outputted from said output port by selectively combining said output from said switching means and data received via said second input port, the mutual order of said data received via said second port being the same when incorporated into said signal as when received via said input port,

wherein said elements are arranged so that:

the first input port of a first one of said switch elements and the first input port of a second one of said switch elements are connected to receive said first signal;

the first input port of a third one of said switch elements and the first input port of a fourth one of said switch elements are connected to receive said second signal;

the output port of said first switch element is connected to the second input port of said third switch element;

the output port of said second switch element is connected to the second input port of said fourth switch element; and

the output ports of said third switch element and said fourth switch element thereby provides said first and second output signal, respectively.

2. An apparatus as claimed in claim 1, wherein the second input port of said first switch element and the second input port of said second switch element are not connected to receive any signals.

3. An apparatus as claimed in claim 1 or 2, wherein each one of said elements is arranged to receive data in essentially equally sized frames via at least one of the input ports of the respective element and to output data in essentially equally sized frames at the output port of the respective element.

4. An apparatus as claimed in any one of the preceding claims, wherein said data is transferred in fixed size time slots.

5. An apparatus as claimed in any one of the preceding claims, wherein the output from said switching means, and said data from said input port, to said selecting means is provided in frames.

6. An apparatus as claimed in any one of the preceding claims, wherein said selecting means is arranged to select, for each time slot to be outputted from said output port, either a time slot received from said switching means or a time slot received from said second input port.

7. An apparatus claimed in any one of the preceding claims, wherein said selecting means is arranged, when selecting the n:th slot of a frame to be outputted from said output port, to select either the n:th slot of a frame received from said switching means or the n:th slot of a frame received from said second input port.

8. An apparatus as claimed in any one of the preceding claims, wherein each one of said switch elements comprises an additional output port (125), wherein data received at the first input port (110) of the respective element is transmitted from said additional output port as received at said first input port, and wherein:

the first input port of said second switch element is connected to receive said first signal by being connected to the additional output port of said first switch element; and

the first input port of said fourth switch element is connected to receive said second signal by being connected to the additional output port of said third switch element.

9. An apparatus for time and space switching data from four or more input signals to four or more output signals, said apparatus including at least four switch elements (500), each having at least four input ports and at least two output ports and comprising:

first switching means (530) arranged to provide for time-and-space-switching of data received from a first one (510) of said input ports to provide an output referring to a first one (550) of said output ports as well as an output referring to a second one (551) of said output ports;

second switching means (531) arranged to provide for time-and-space-switching of data received from a third one (511) of said input ports to provide an output referring to said first output port (550) as well as an output referring to said second output port (551);

first selecting means (540) for defining a signal to be outputted from said first output port (550) by selectively combining the output from said first switching means (530) that refers to said first output port (550), the output from said second switching means (531) that

refers to said first output port (550), and data received via a second one (520) of said input ports, the mutual order of said data received via said second port being the same when incorporated into said signal as when received via said input port; and

second selecting means (541) for defining a signal to be outputted from said second output port (551) by selectively combining the output from said first switching means (530) that refers to said second output port (551), the output from said second switching means (531) that refers to said second output port (551), and data received via a fourth one (521) of said input ports, the mutual order of said data received via said fourth port being the same when incorporated into said signal as when received via said fourth input port,

wherein said elements are arranged so that:

the first input port of a first one of said switch elements and the first input port of a second one of said switch elements are connected to receive a first one of said input signals;

the third input port of said first switch element and the third input port of said second switch element are connected to receive a second one of said input signals;

the first input port of a third one of said switch elements and the first input port of a fourth one of said switch elements are connected to receive a third one of said input signals;

the third input port of said third switch element and the third input port of said fourth switch element are connected to receive a fourth one of said input signals;

the first and second output port of said first switch element is connected to the second and fourth input port, respectively, of said third switch element;

the first and second output port of said second switch element is connected to the second and fourth input port, respectively, of said fourth switch element;

the first and second output port of said third switch element thereby provides a first and a second one, respectively, of said four or more output signals and the first and second output port of said fourth switch element thereby provides a third and a fourth one, respectively, of said four or more output signals.

10. An apparatus as claimed in claim 9, wherein the second and fourth input port of said first switch element and the second and fourth input port of said second switch element are not connected to receive any signals.

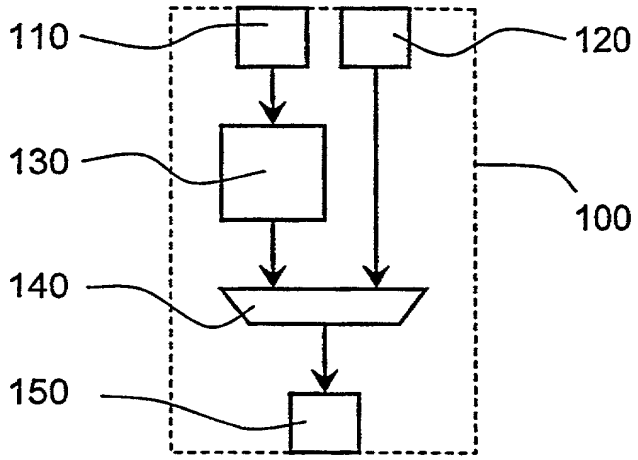
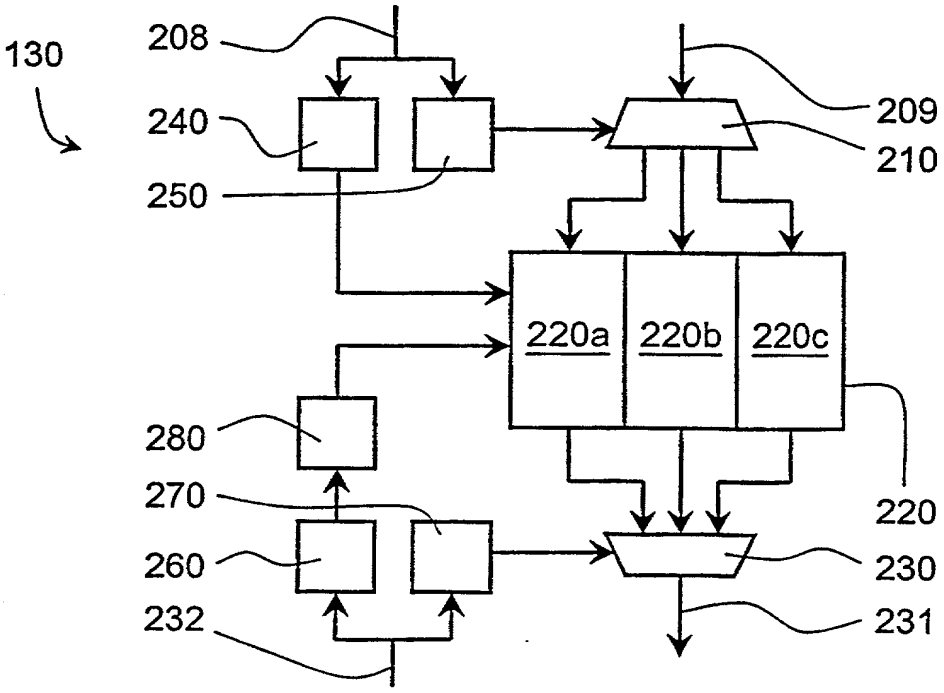

110
120
130
100
140
150

FIG. 1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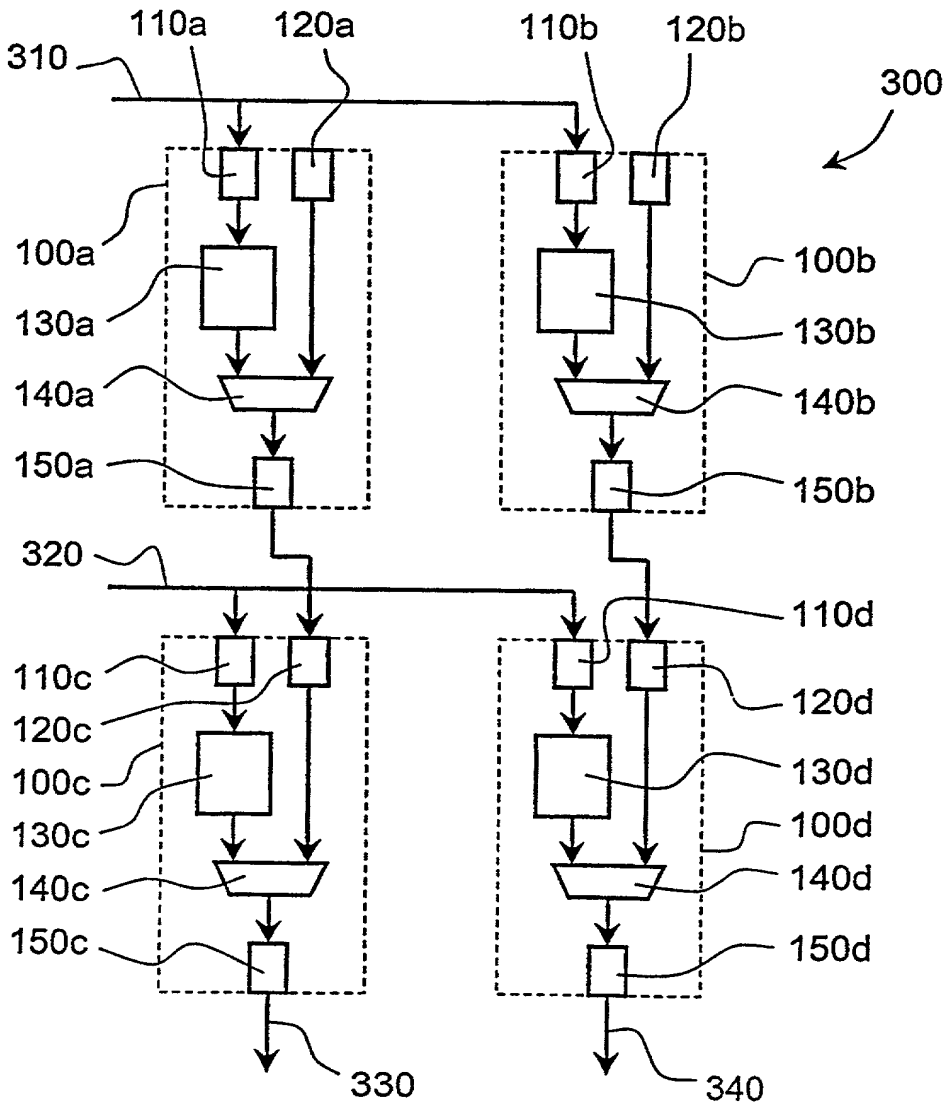
250
209
210
220a
220b
220c
280
270
260
232
220
230
231

FIG. 2


110a
120a
110b
120b
310
300
100a
130a
140a
150a
100b
130b
140b
150b
320
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150c
120d
130d
100d
140d
150d
330
340

FIG. 3

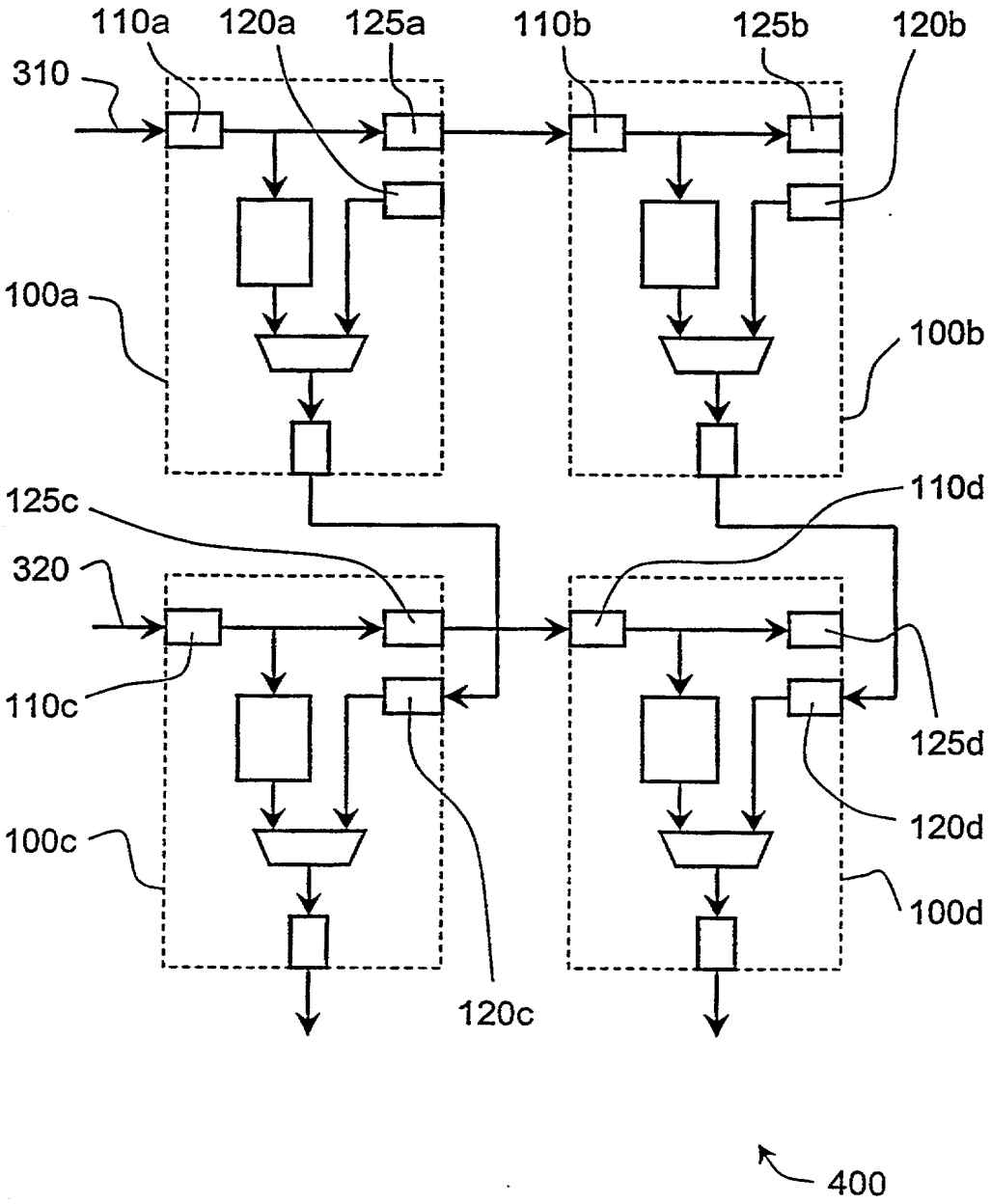
110a
120a
125a
110b
125b
120b
310
100a
100b
125c
110d
320
110c
125d
120d
100c
100d
120c
400

FIG. 4

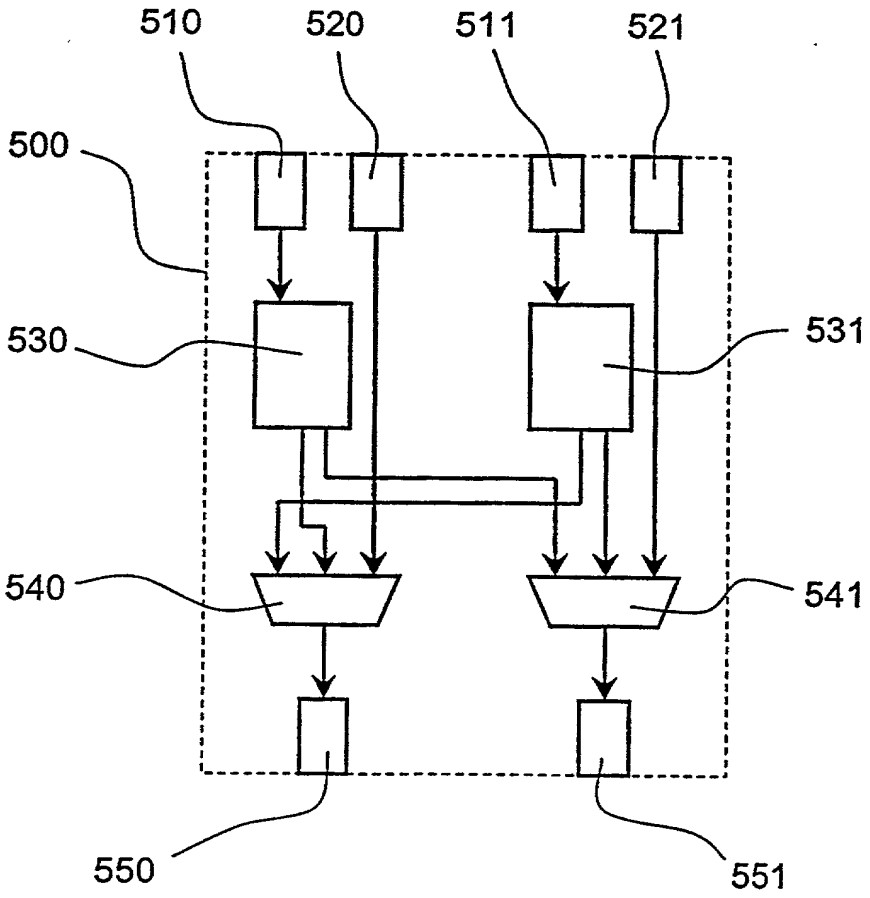

FIG. 5

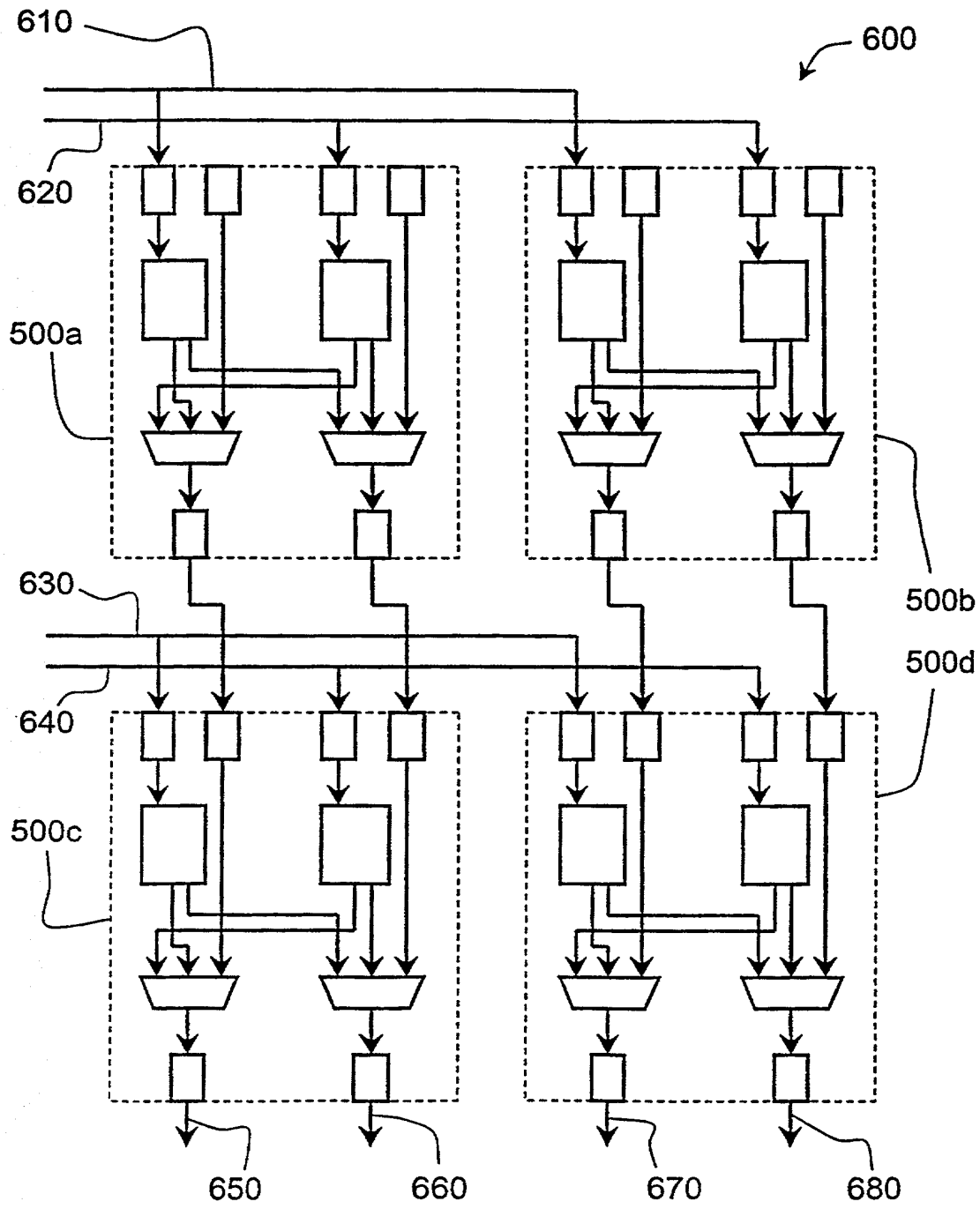

FIG. 6

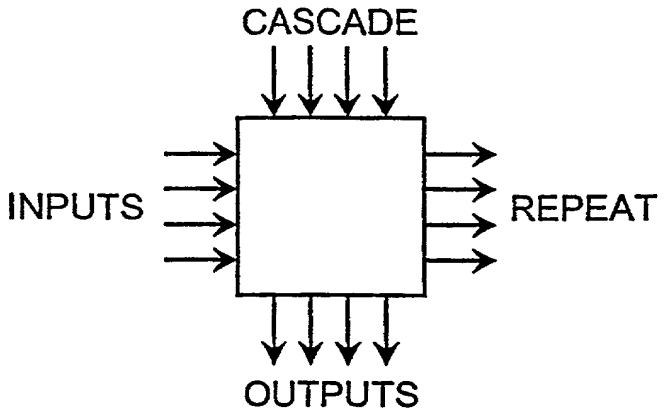

FIG. 7A

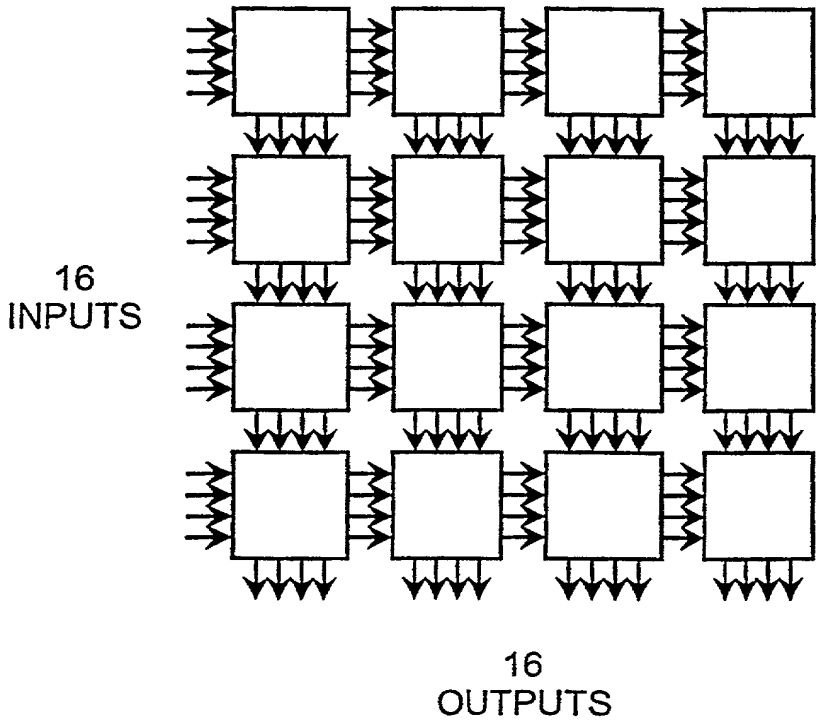

FIG. 7B

DECLARATION FOR NON-PROVISIONAL PATENT APPLICATION*

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below at 201 et seq. beneath my name.

I believe I am the original, first and sole inventor if only one name is listed at 201 below, or an original, first and joint inventor if plural names are listed at 201 et seq. below, of the subject matter which is claimed and for which a patent is sought on the invention entitled

SWITCH APPARATUS

and for which a patent application:
☐ is attached hereto and includes amendment(s) filed on *(if applicable)*
☐ was filed in the United States on as Application No. *(for declaration not accompanying application)*
with amendment(s) filed on *(if applicable)*
☒ was filed as PCT international Application No. PCT/SE00/00850 on May 3, 2000 and was amended under PCT Article 19 on *(if applicable)*

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
9901607-3	Sweden	4 May 1999	YES ☒ NO ☐
PCT/SE00/00850	PCT	3 May 2000	YES ☒ NO ☐
			YES ☐ NO ☐

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

PROVISIONAL APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NON-PROVISIONAL APPLICATION SERIAL NO.	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED

* for use only when the application is assigned to a company, partnership or other organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1-00

201

FULL NAME OF INVENTOR	LAST NAME: Danielson	FIRST NAME: Magnus	MIDDLE NAME:
RESIDENCE & CITIZENSHIP	CITY: Stocksund	STATE OR FOREIGN COUNTRY: Sweden SEK	COUNTRY OF CITIZENSHIP: Sweden
POST OFFICE ADDRESS	STREET: Kyrkvägen 3 A	CITY: Stocksund	STATE OR COUNTRY: Sweden / ZIP CODE: SE-182 74
	SIGNATURE OF INVENTOR 201		DATE: 20/11 -2001

2-00

202

FULL NAME OF INVENTOR	LAST NAME: Roos	FIRST NAME: Joachim	MIDDLE NAME:
RESIDENCE & CITIZENSHIP	CITY: Nacka	STATE OR FOREIGN COUNTRY: Sweden SEK	COUNTRY OF CITIZENSHIP: Sweden
POST OFFICE ADDRESS	STREET: Kristinedalsvägen	CITY: Nacka	STATE OR COUNTRY: Sweden / ZIP CODE: SE-131 46
	SIGNATURE OF INVENTOR 202		DATE: 15 NOVEMBER 2001

203

FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
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POST OFFICE ADDRESS	STREET	CITY	STATE OR COUNTRY / ZIP CODE
	SIGNATURE OF INVENTOR 203		DATE

204

FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS	STREET	CITY	STATE OR COUNTRY / ZIP CODE
	SIGNATURE OF INVENTOR 204		DATE

205

FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS	STREET	CITY	STATE OR COUNTRY / ZIP CODE
	SIGNATURE OF INVENTOR 205		DATE

POWER OF ATTORNEY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Danielson et al.

Application No.: TBA	Group Art Unit: TBA
Filed: October 22, 2001	Examiner: TBA
For: SWITCH APPARATUS	Attorney Docket No.: 10806-013

POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR(S) UNDER 37 C.F.R. 3.71

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned assignee of the entire interest in the above-identified subject application hereby appoints: Berj A. Terzian (Reg. No. 20060), David Weild, III (Reg. No. 21094), Jonathan A. Marshall (Reg. No. 24614), Barry D. Rein (Reg. No. 22411), Stanton T. Lawrence, III (Reg. No. 25736), Charles E. McKenney (Reg. No. 22795), Philip T. Shannon (Reg. No. 24278), Francis E. Morris (Reg. No. 24615), Charles E. Miller (Reg. No. 24576), Gidon D. Stern (Reg. No. 27469), John J. Lauter, Jr. (Reg. No. 27814), Brian M. Poissant (Reg. No. 28462), Brian D. Coggio (Reg. No. 27624), Rory J. Radding (Reg. No. 28749), Stephen J. Harbulak (Reg. No. 29166), Donald J. Goodell (Reg. No. 19766), Thomas E. Friebel (Reg. No. 29258), Laura A. Coruzzi (Reg. No. 30742), Jennifer Gordon (Reg. No. 30753), Geraldine F. Baldwin (Reg. No. 31232), Victor N. Balancia (Reg. No. 31231), Samuel B. Abrams (Reg. No. 30605), Steven I. Wallach (Reg. No. 35402), Marcia H. Sundeen (Reg. No. 30893), Paul J. Zegger (Reg. No. 33821), Edmond R. Bannon (Reg. No. 32110), Bruce J. Barker (Reg. No. 33291), Adriane M. Antler (Reg. No. 32605), Thomas G. Rowan (Reg. No. 34419), James G. Markey (Reg. No. 31636), Thomas D. Kohler (Reg. No. 32797), Scott D. Stimpson (Reg. No. 33607), Gary S. Williams (Reg. No. 31066), Ann L. Gisolfi (Reg. No. 31956), Todd A. Wagner (Reg. No. 35399), Scott B. Familant (Reg. No. 35514), Kelly D. Talcott (Reg. No. 39582), Francis D. Cerrito (Reg. No. 38100), Anthony M. Insogna (Reg. No. 35203), Brian M. Rothery (Reg. No. 35340), Brian D. Siff (Reg. No. 35679), Alan Tenenbaum (Reg.

No. 34939), Michael J. Lyons (Reg. No. 37386), Garland T. Stephens (Reg. No. 37242), William J. Sipio (Reg. No. 34514), Nikolaos C. George (Reg. No. 39201), Stephen S. Rabinowitz (Reg. No. 40286), Ognjan V. Shentov (Reg. No. 38051), and Kenneth L. Stein (Reg. No. 38704), all of Pennie & Edmonds LLP, whose addresses are 1155 Avenue of the Americas, New York, New York 10036, 1667 K Street N.W., Washington, DC 20006 and 3300 Hillview Avenue, Palo Alto, CA 94304, all of Pennie & Edmonds LLP (PTO Customer No. 20583), as its attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. 3.71, provided that, if any one of these attorneys ceases being affiliated with the law firm of Pennie & Edmonds LLP as partner, counsel, or employee, then the appointment of that attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated.

An assignment of the entire interest in the above-identified subject application:

[ ] was recorded on _____ at reel/frame _/_____.

[ ] is submitted herewith for recording.

[x] A copy of an assignment of the entire interest in the above-identified subject application is submitted herewith. The assignment will be duly recorded.

Please direct all correspondence for this application to customer no. 20583.

ASSIGNEE: NET INSIGHT AB

Signature: _____

Typed Name: TOMAS DUFFY

Position/Title: CEO

Address: BOX 42093
SE-126 14 STOCKHOLM
SWEDEN

Date: December 7, 2001

ASSIGNMENT **JOINT**

WHEREAS, WE, Magnus Danielson, and Joachim Roos, ASSIGNORS, citizens of Sweden, residing at Kyrkvägen 3A, SE-182 74 Stocksund, Sweden, and Kirstinedalsvägen 32 B, SE-131 46 Nacka, Sweden, respectively, are the inventors of the invention in SWITCH APPARATUS for which we have executed an application for a Patent of the United States

☒ which is identified by Pennie & Edmonds LLP docket no. 10806-013
☒ which was filed on October 22, 2001, Application No. TBA

and WHEREAS, Net Insight AB, ASSIGNEE, a corporation organized under the laws of Sweden, is desirous of obtaining our entire right, title and interest in, to and under the said invention and the said application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to us in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, we, the said ASSIGNORS, have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, our entire right, title and interest in, to and under the said invention, and the said United States application and all divisions, renewals and continuations thereof, and all Patents of the United States which may be granted thereon and all reissues and extensions thereof; and all applications for industrial property protection, including, without limitation, all applications for patents, utility models, and designs which may hereafter be filed for said invention in any country or countries foreign to the United States, together with the right to file such applications and the right to claim for the same the priority rights derived from said United States application under the Patent Laws of the United States, the International Convention for the Protection of Industrial Property, or any other international agreement or the domestic laws of the country in which any such application is filed, as may be applicable; and all forms of industrial property protection, including, without limitation, patents, utility models, inventors' certificates and designs which may be granted for said invention in any country or countries foreign to the United States and all extensions, renewals and reissues thereof;

AND WE HEREBY authorize and request the Commissioner of Patents and Trademarks of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents or other evidence or forms of industrial property protection on applications as aforesaid, to issue the same to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant and agree that we have full right to convey the entire interest herein assigned, and that we have not executed, and will not execute, any agreement in conflict herewith.

AND WE HEREBY further covenant and agree that we will communicate to the said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said invention, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing, reissue and foreign applications, make all rightful oaths, and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper protection for said invention in all countries.

IN TESTIMONY WHEREOF, We hereunto set our hands and seals the day and year set opposite our respective signatures.

Date 20/11-2001, 2001 _____ L.S.
Magnus Danielson (Signature)

On this 20 day of November, 2001, before me, a witness, personally appeared Magnus Danielson, to me known and known to me to be the person of that name, who signed the foregoing instrument, and he acknowledged the same to be his free act and deed.

_____
Witness

Date 15 NOVEMBER, 2001 _____ L.S.
Joachim Roos (Signature)

On this 15 day of November, 2001, before me, a witness, personally appeared Joachim Roos, to me known and known to me to be the person of that name, who signed the foregoing instrument, and he acknowledged the same to be his free act and deed.

_____
Witness